

FIG.1
PRIOR ART

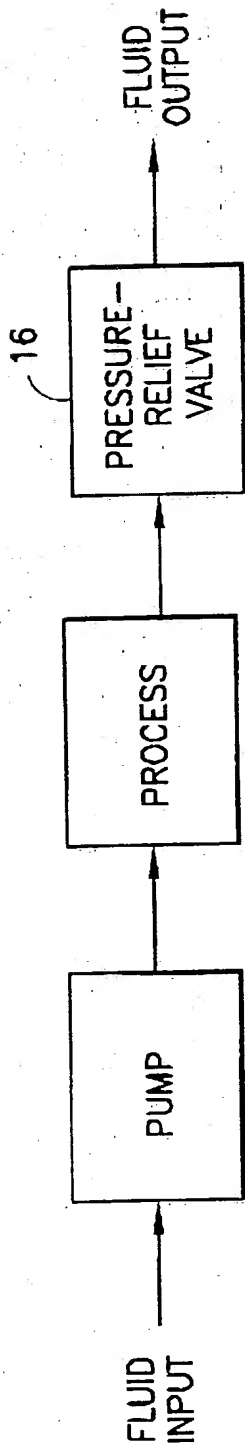


FIG. 2
PRIOR ART

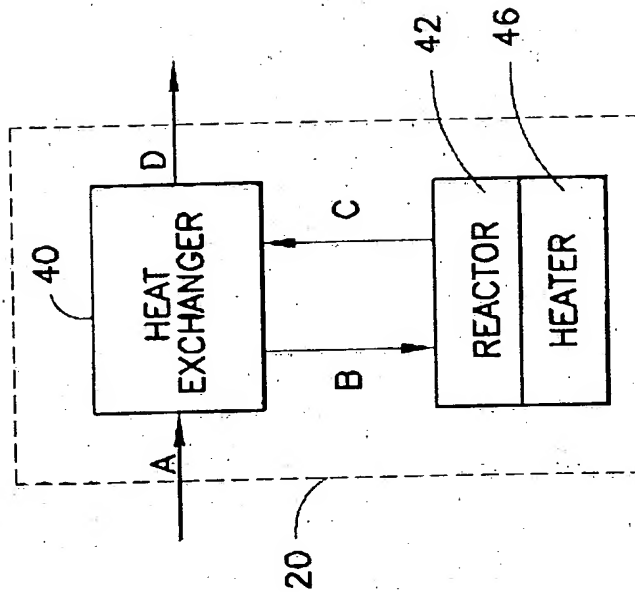
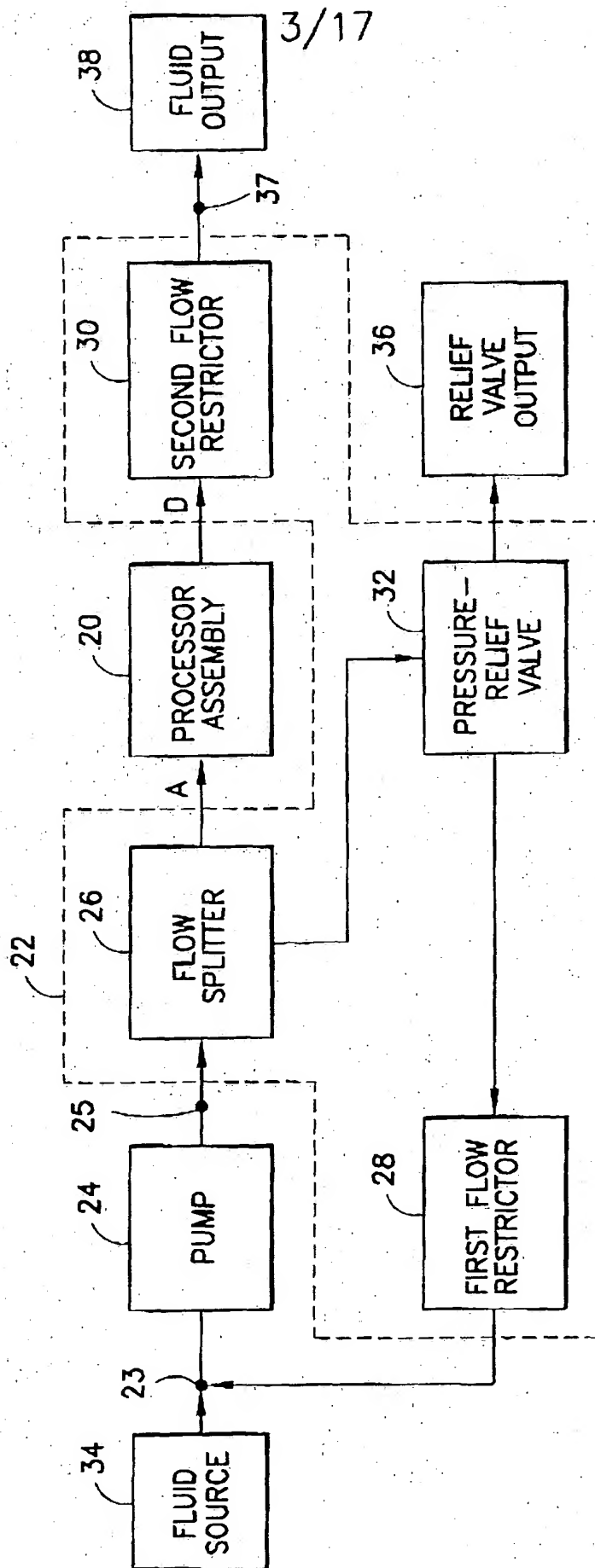


FIG. 4



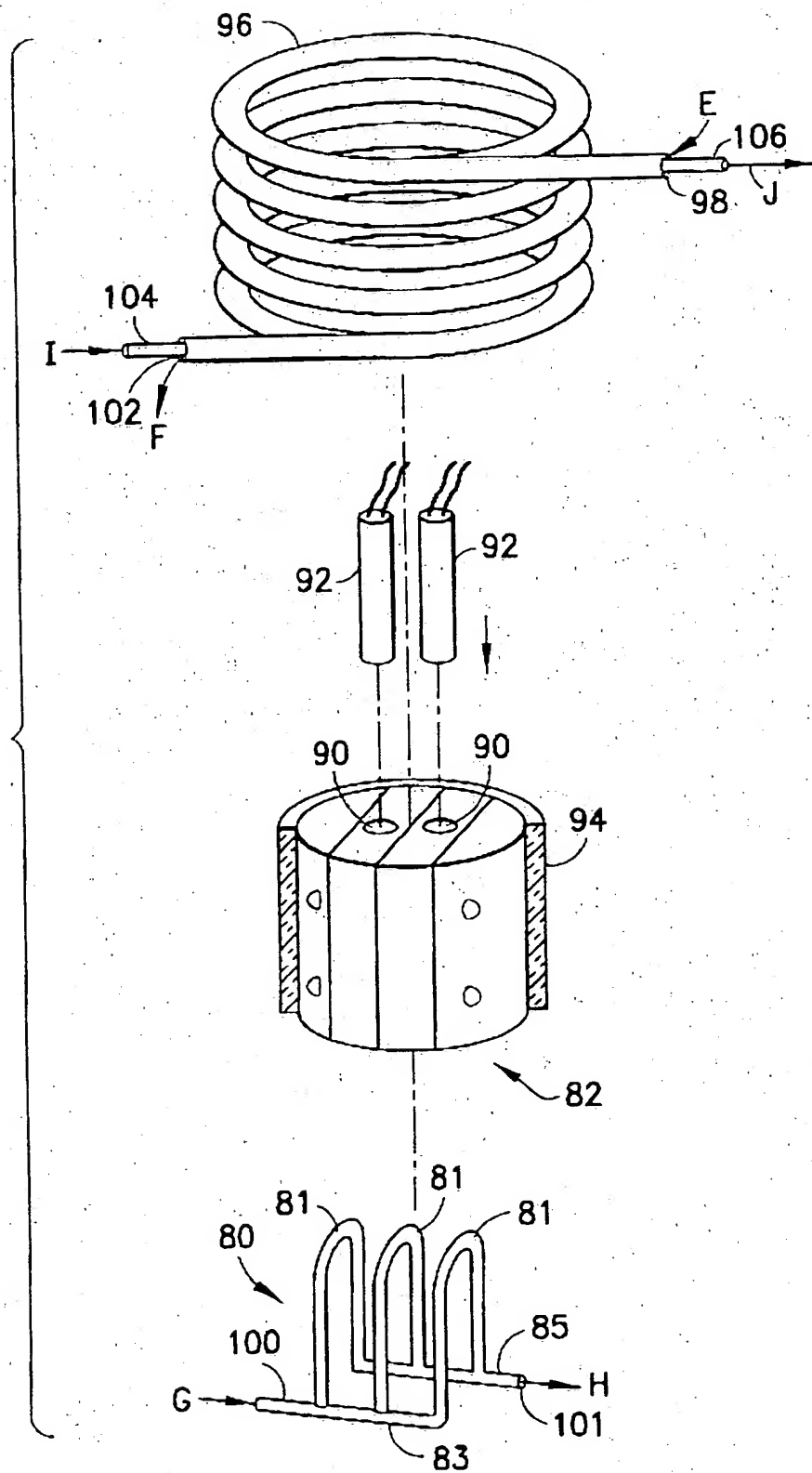


FIG. 5A

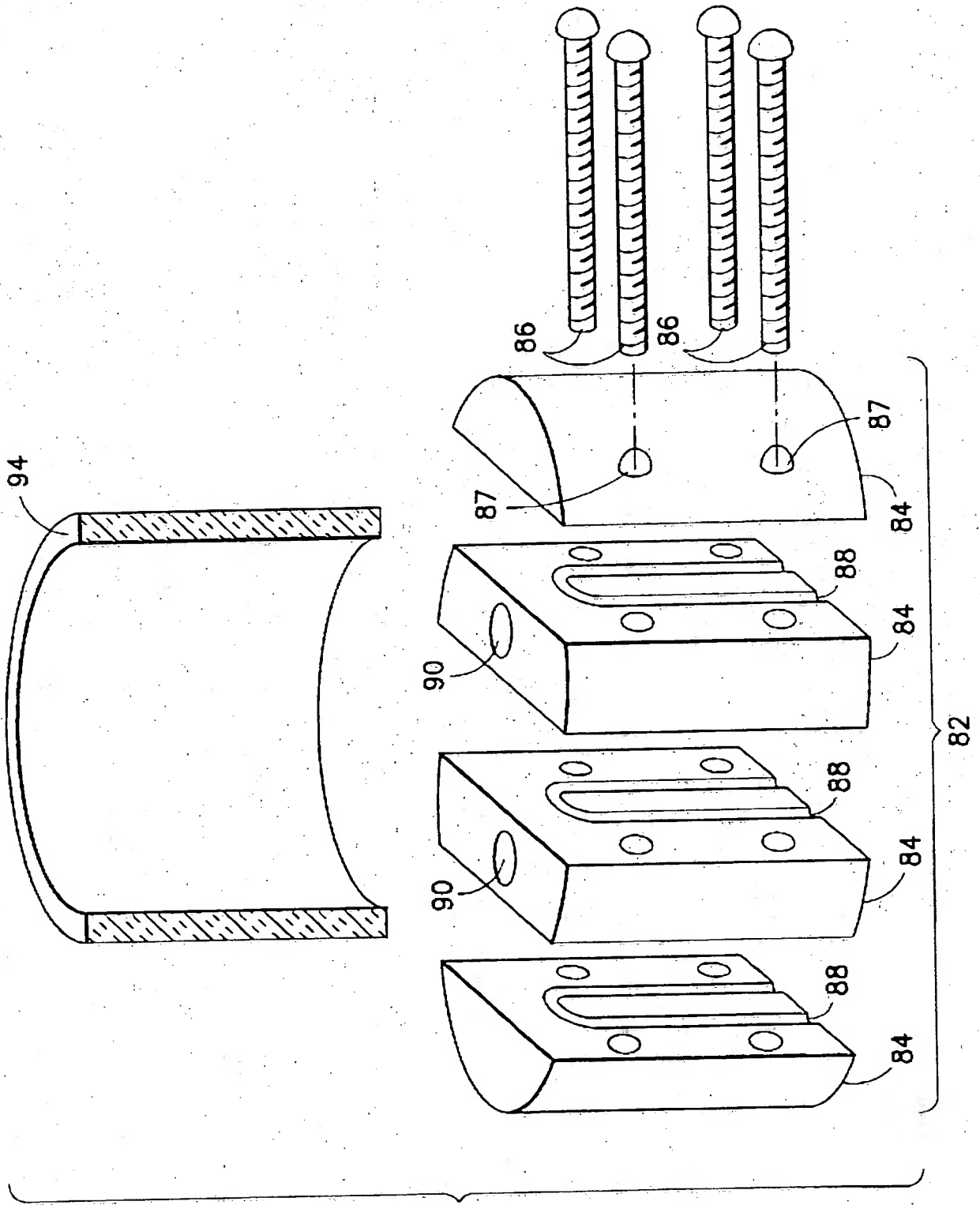


FIG. 5B

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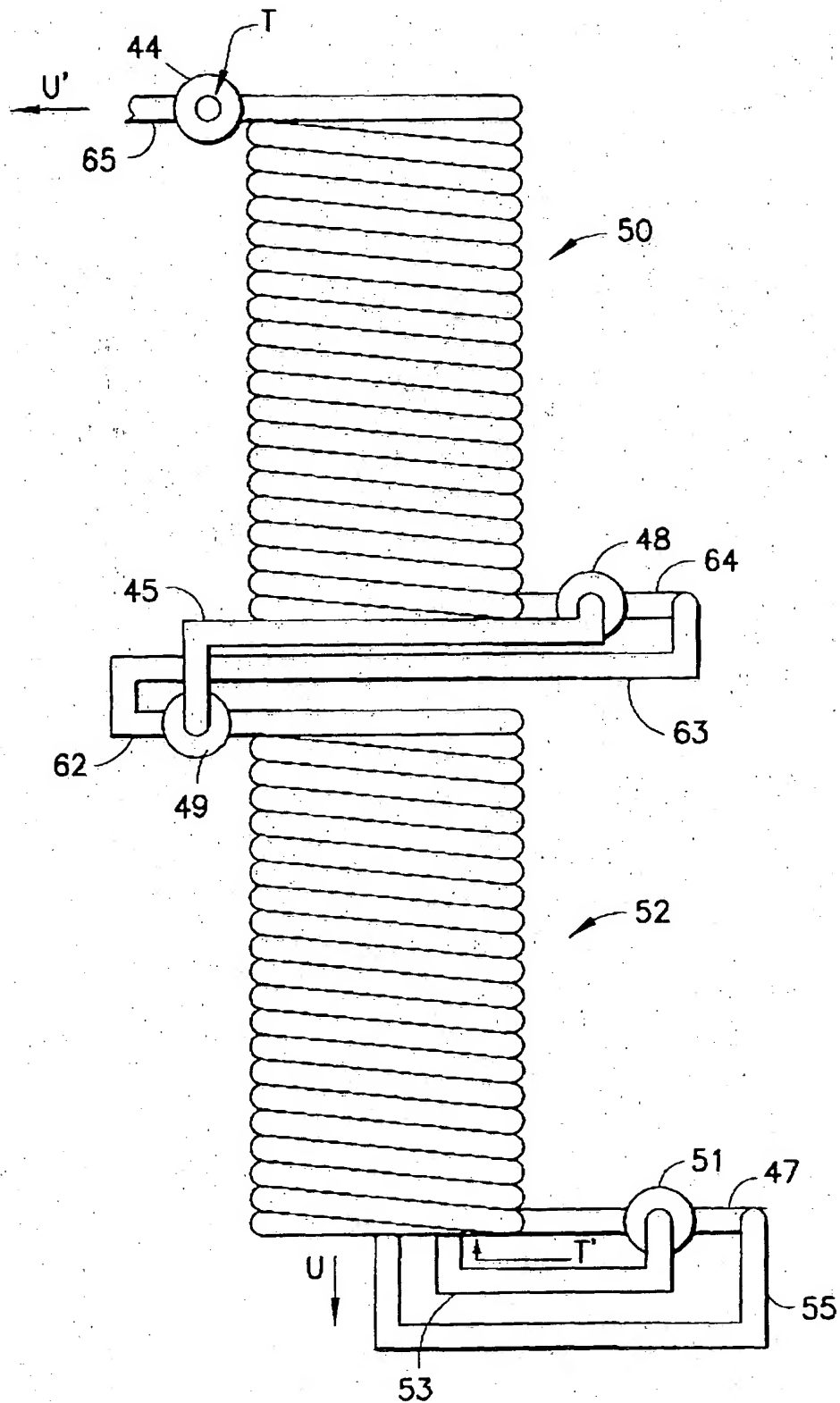


FIG.5C

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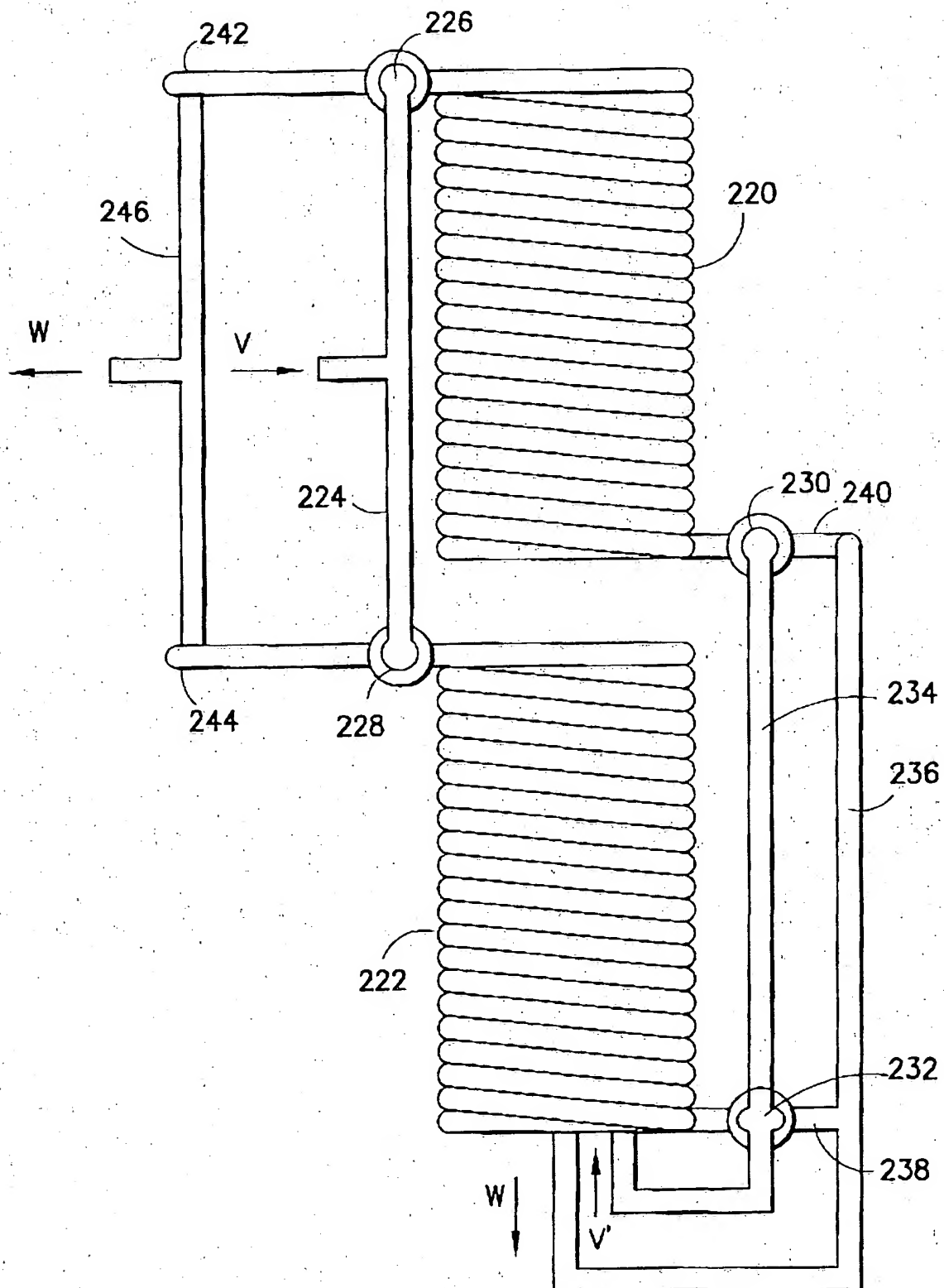


FIG.5D

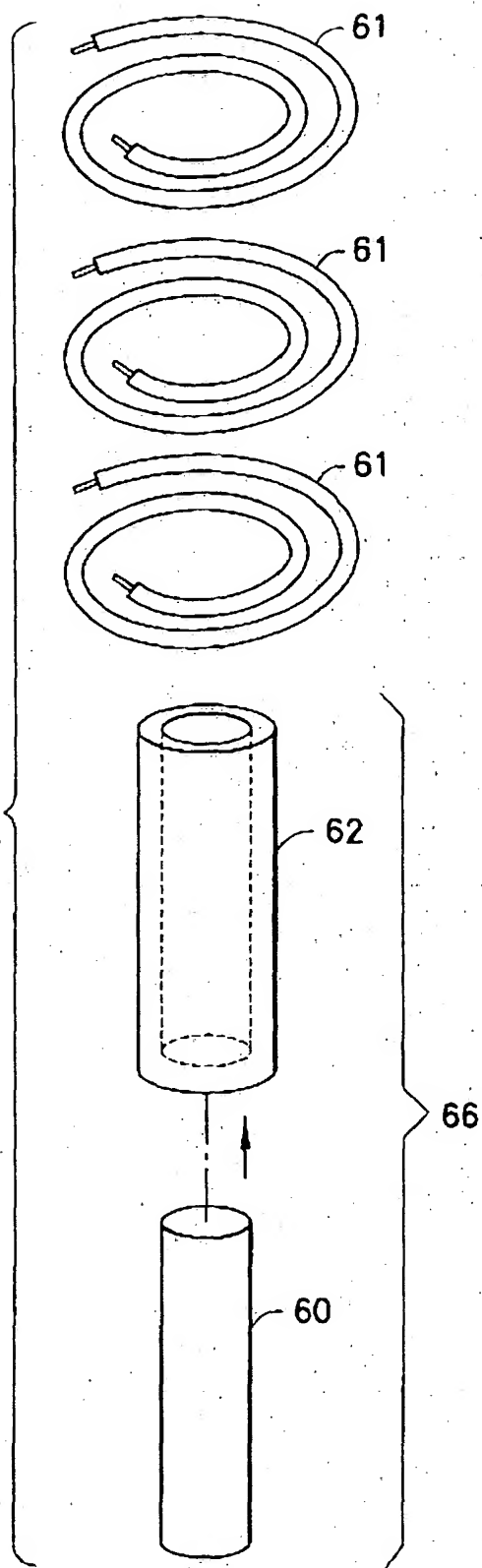


FIG. 6A

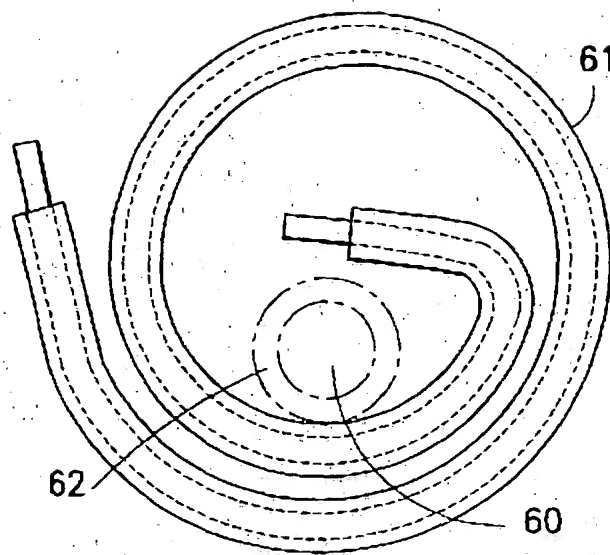


FIG. 6B

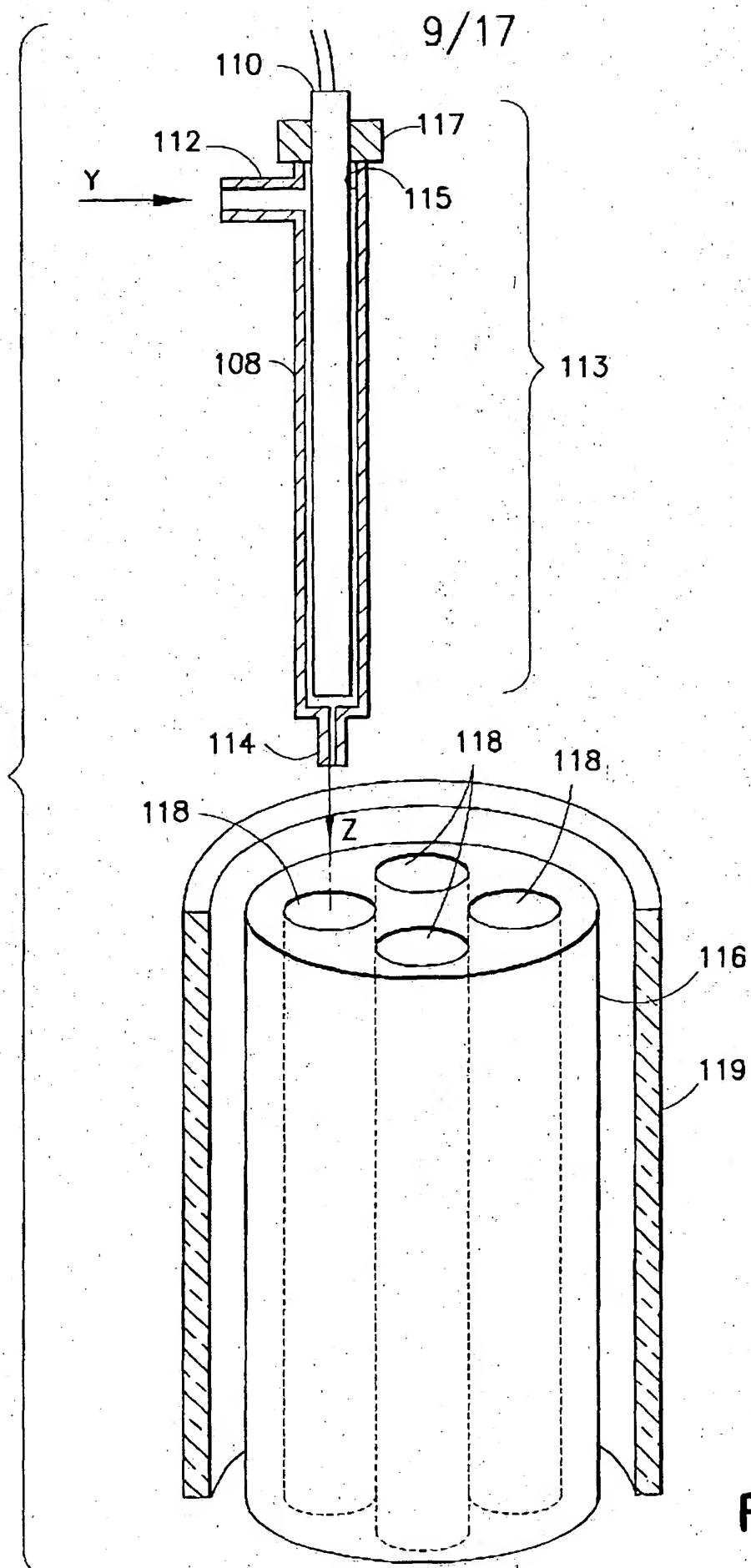


FIG.7

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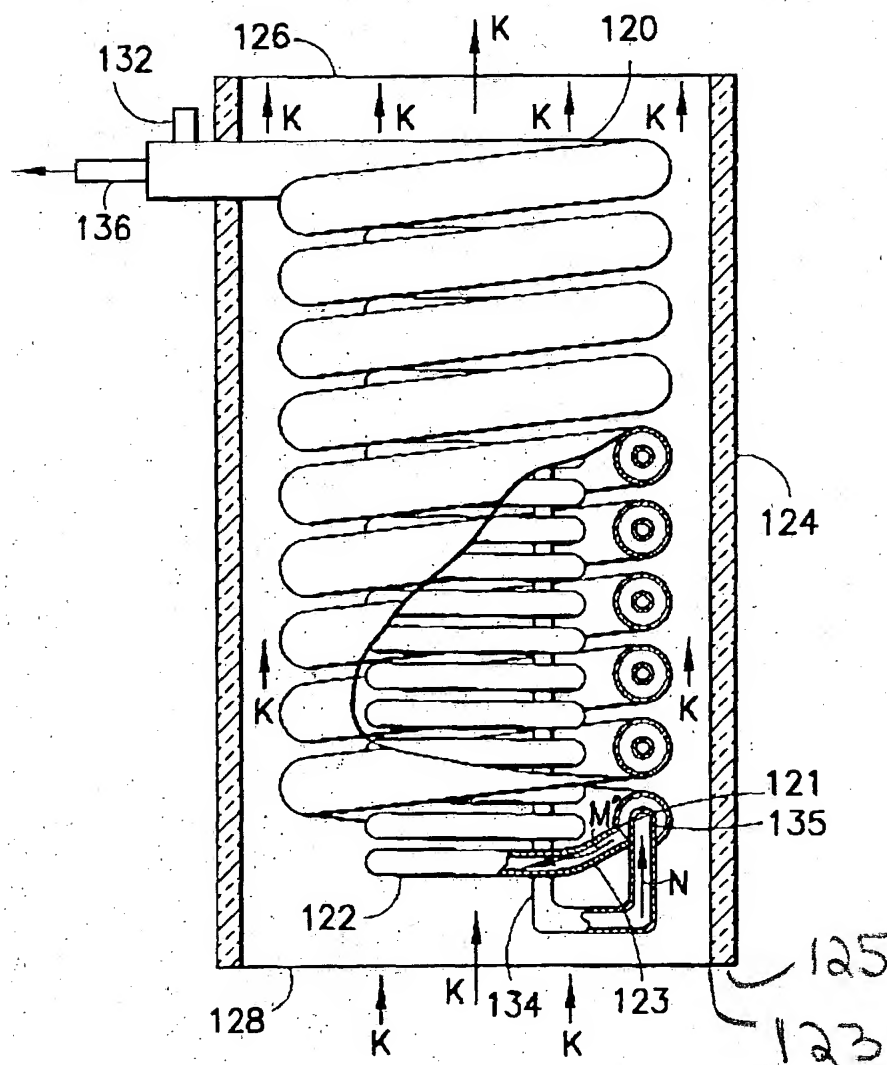


FIG. 8A

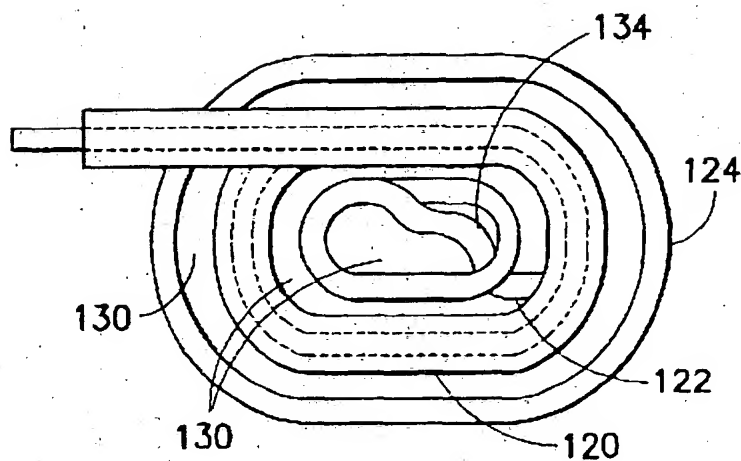


FIG. 8B

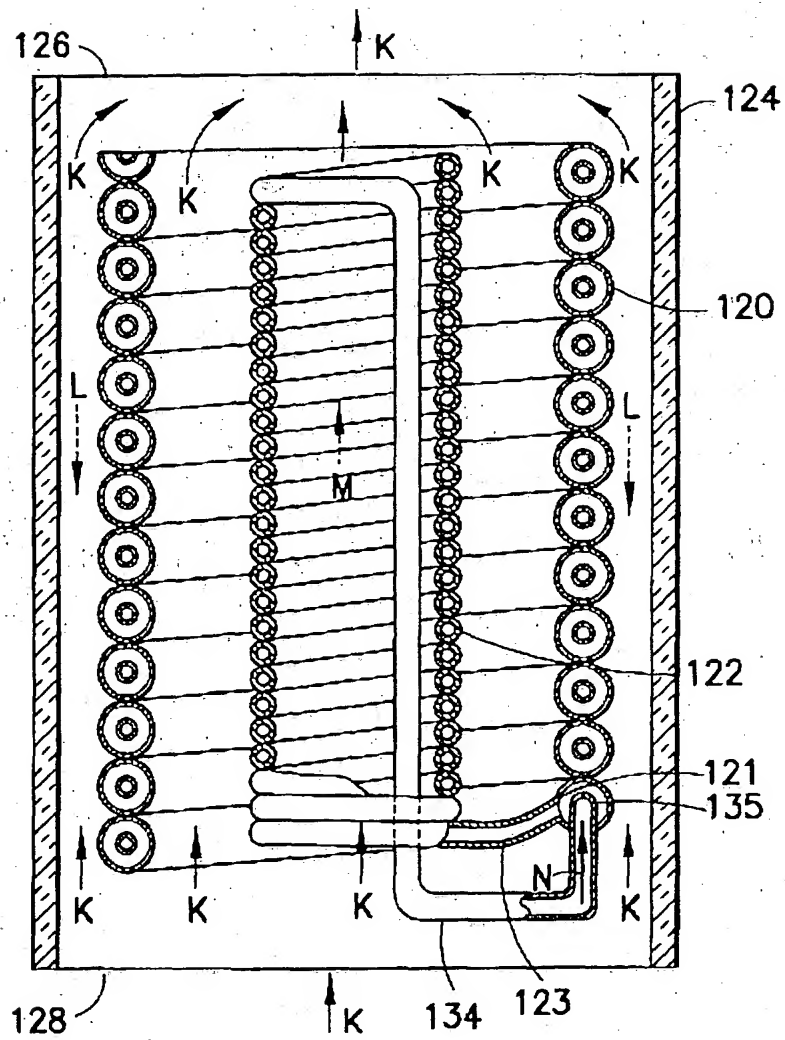


FIG.8C

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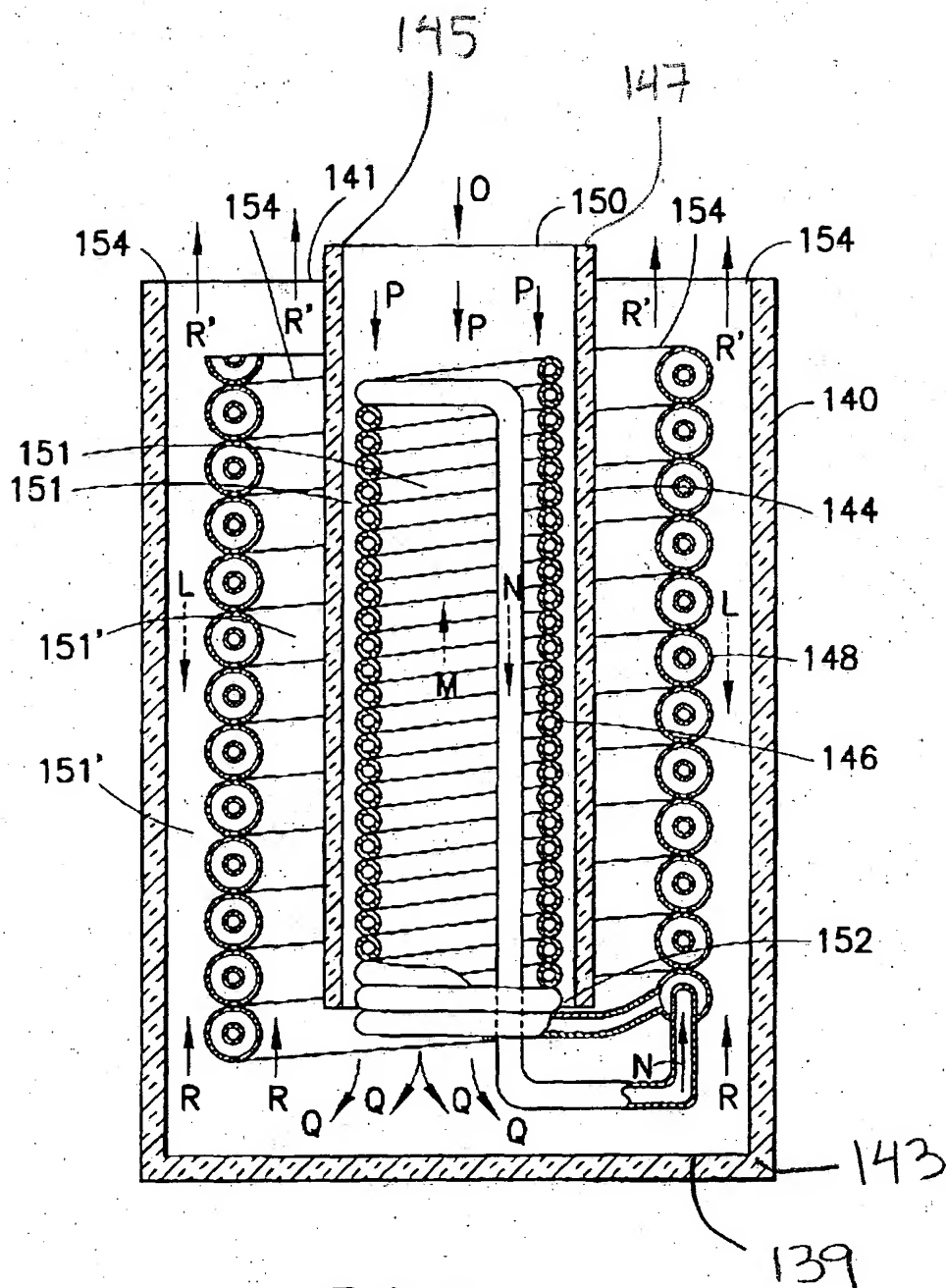


FIG.9

PROCESSOR ASSEMBLY

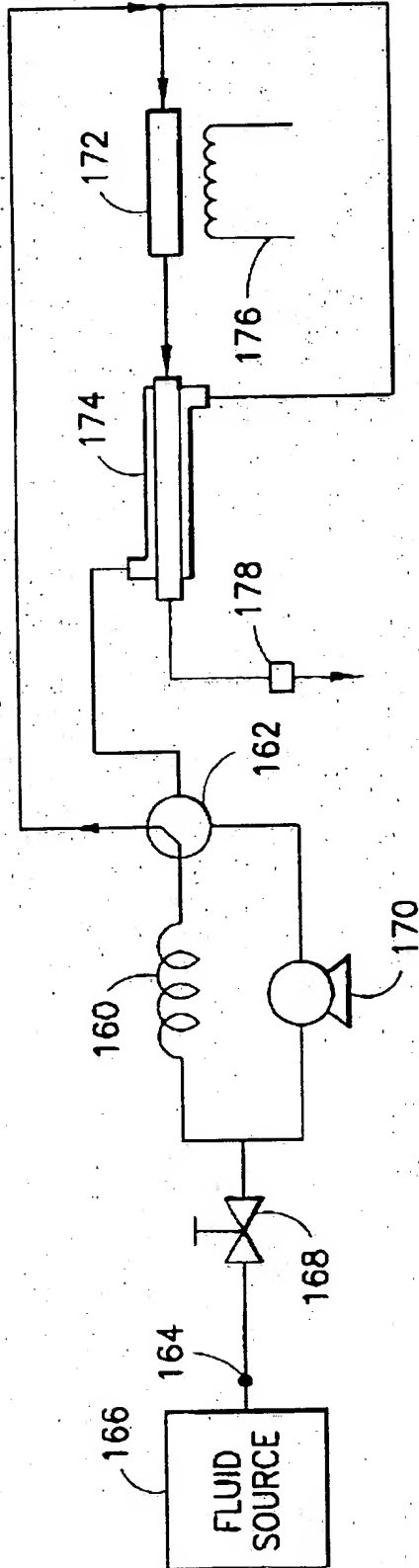


FIG. 10A

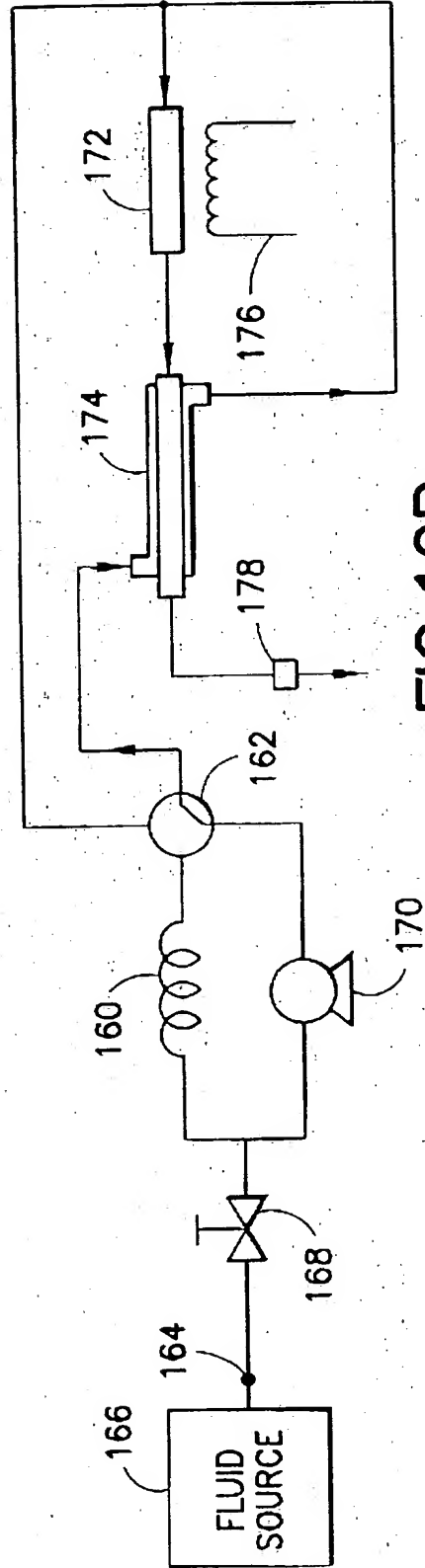


FIG. 10B

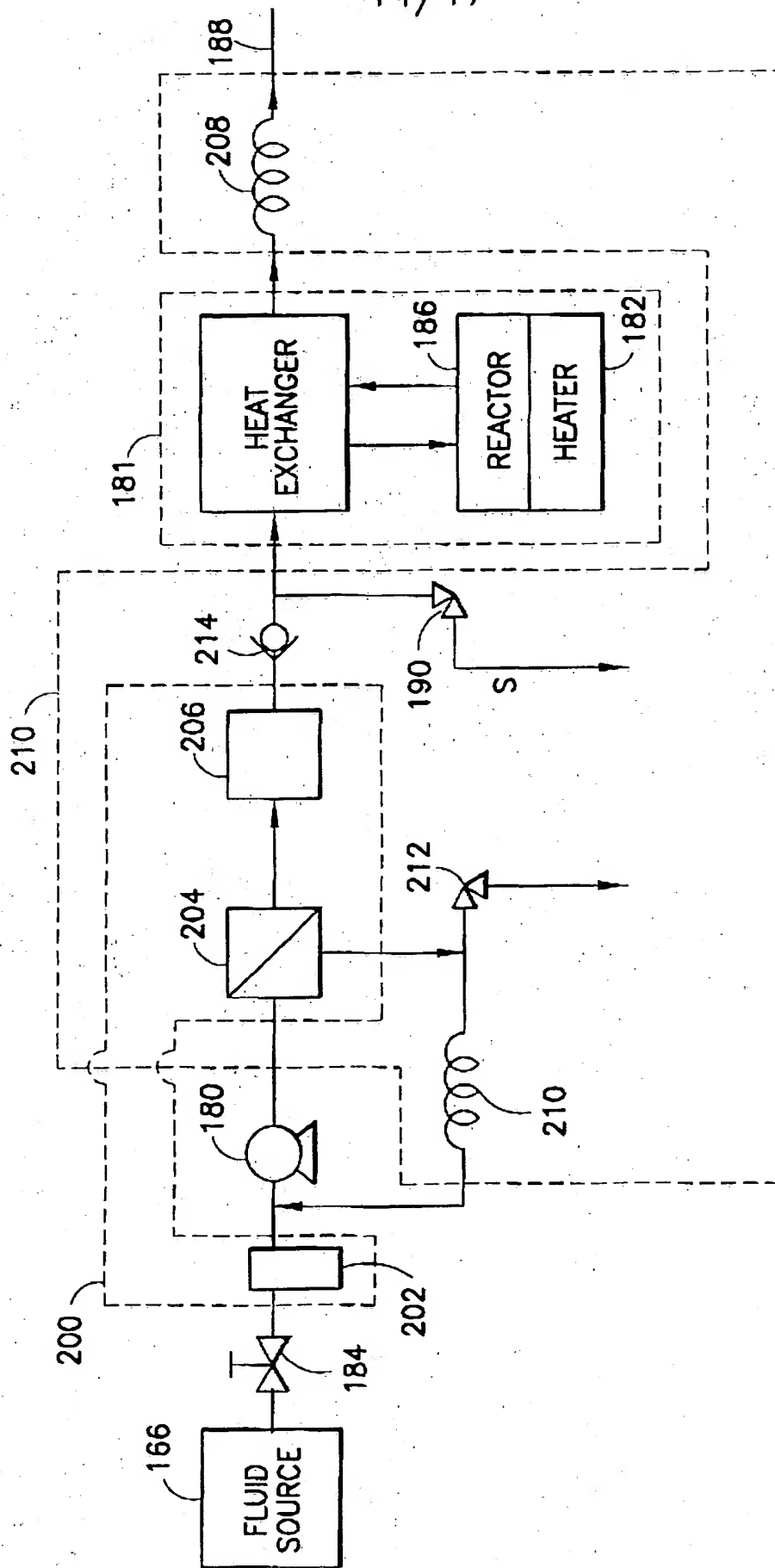


FIG.11A

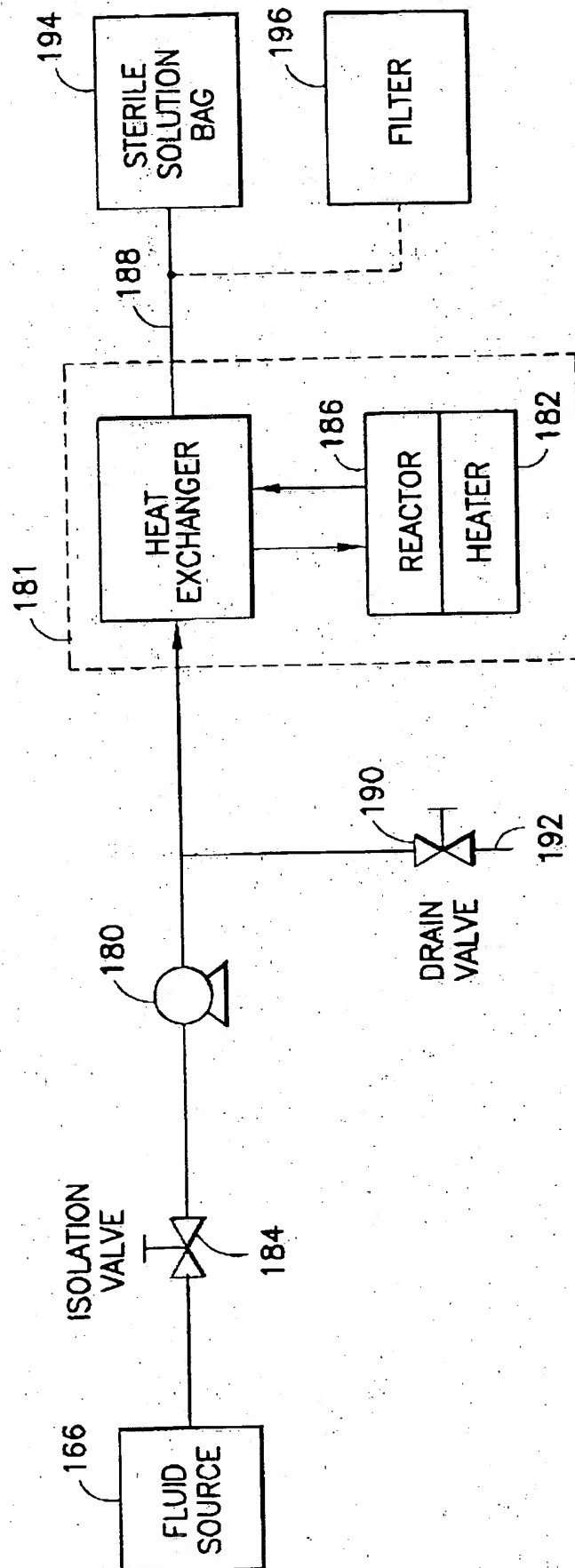


FIG. 11B

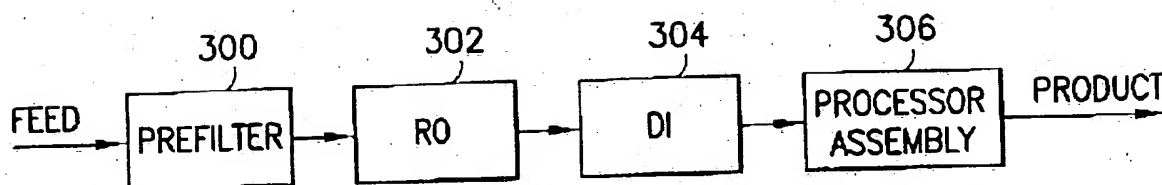


FIG. 12A

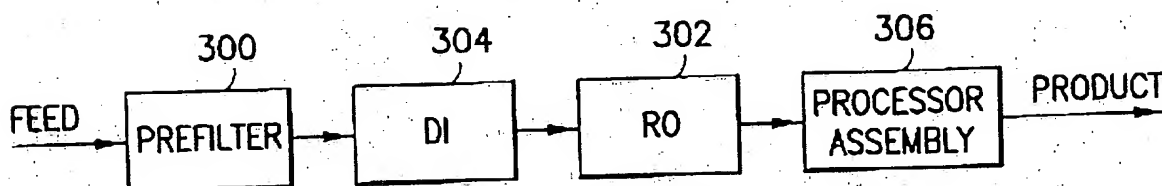


FIG. 12B

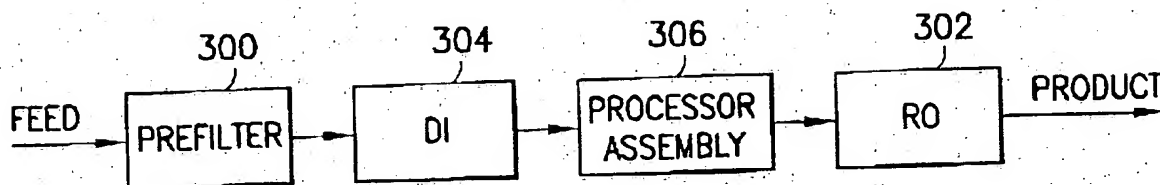


FIG. 12C

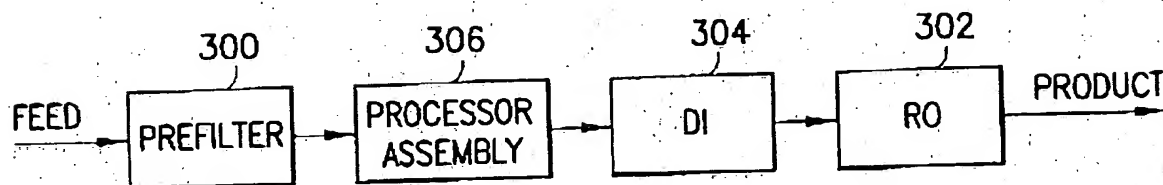


FIG. 12D

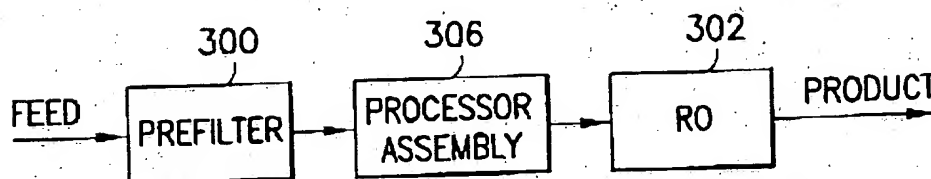


FIG. 12E

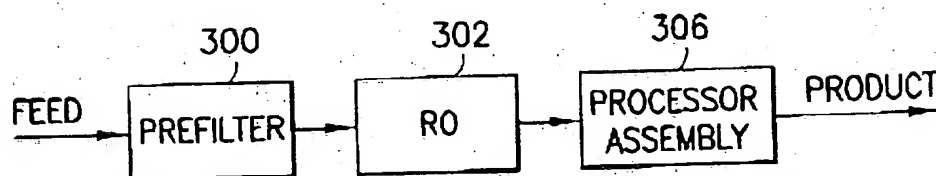


FIG. 12F

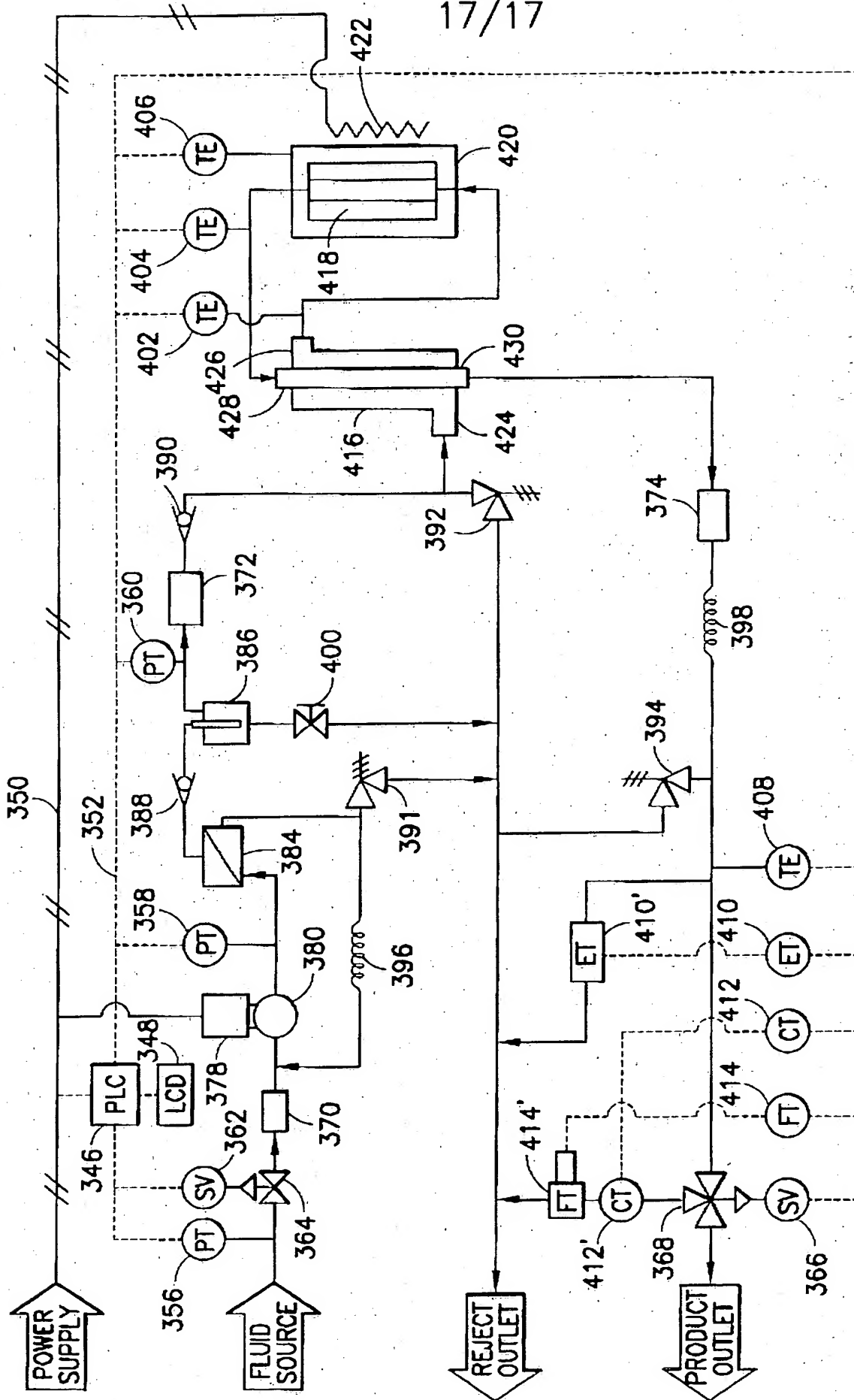


FIG. 13